11 (Amended). A printed circuit board comprising a substrate and, built thereon, a circuit comprised of a copper film,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

12 (Amended). A printed circuit board comprising a substrate formed with a conductor circuit, an interlayer resin insulating layer thereon and a conductor circuit comprised of a copper film on said interlayer resin insulating layer and having via holes by which said conductor circuits are interconnected,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

13 (Amended). The printed circuit board according to Claim 11 wherein said copper film has an elongation of not less than 7%.

22 (Amended). A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, thereon, a conductor circuit comprising at least an electroless plated film, wherein said electroless plated film has a stress of 0 to +10 kg/mm^2.

23 (Amended). A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, built thereon by semi-additive process, a conductor circuit comprising at least an electroless plated film,

wherein said roughened surface comprises convex areas and concave areas, and said electroless plated film is complementary to said roughened surface with

said electroless plated film in convex areas of said roughened surface being relatively greater in thickness than said electroless plated film in concave areas of said roughened surface.

24 (Amended). A printed circuit board comprising a substrate board formed with a lower-layer conductor circuit and, built thereon, an upper-layer conductor circuit through the intermediary of an interlayer resin insulating layer, with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes,

wherein said upper-layer conductor circuit comprises at least an electroless plated film, said interlayer resin insulating layer is provided with a roughened surface, with said electroless plated film being complementary to said roughened surface, and

said interlayer resin insulating layer and said via holes are provided with the same electroless plated film, with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the thickness of said electroless plated film on said interlayer resin insulating layer.

25 (Amended). A printed circuit board comprising a resin insulating substrate board and thereon a conductor circuit comprising at least an electroless plated film,

wherein said electroless plated film is a copper film, and comprises at least one metal species selected from the group consisting of nickel, iron and cobalt.

32 (Amended). A multilayer printed circuit board comprising a core board having a conductor circuit and, over said conductor circuit, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board comprises a copper-clad laminate, said conductor circuit comprises a copper foil of said copper-clad laminate and a plated metal layer,

the thickness of said conductor circuit is not greater by more than 10 μm than the thickness of said conductor layer on said interlayer resin insulating layer, and

the thickness of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer.

37 (Amended). A multilayer printed circuit board comprising a core board and on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein said conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, said via holes are formed immediately over said plated-through holes in the manner of plugging the through holes in said plated-through holes and are interconnected with said plated-through holes.

40 (Amended). A multilayer printed circuit board comprising a core board and on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed immediately over said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

41 (Amended). A multilayer printed circuit board comprising a core board and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and said plated-through holes are filled with a filler, with the surfaces of said filler which are

exposed from said plated-through holes being covered with said conductor layer provided with lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said lower-layer via holes being interconnected with said upper-layer via holes.

42 (Amended). A multilayer printed circuit board comprising a core board and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer and a conductor layer thereon, wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed to plug through holes of said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

44 (Amended). The multilayer printed circuit board according to any of Claims 40 to 43, wherein said lower-layer via holes are filled with metal.

Please add the following new claims:

48 (New). The circuit board according to Claim 9, wherein said copper film is formed by constant-voltage pulse plating technique.

49 (New). The printed circuit board according to Claim 11, wherein said copper film is formed by constant-voltage pulse plating technique.

50 (New). The printed circuit board according to Claim 12, wherein said copper film has an elongation of not less than 7%.

51 (New). The printed circuit board according to Claim 12, wherein said copper film is formed by constant-voltage pulse plating technique.

52 (New). The printed circuit board according to Claim 22, wherein said electroless plated film is formed from an electroless plating solution comprising tartaric acid or a salt thereof.

53 (New). The printed circuit board according to Claim 23, wherein said roughened surface comprises a primary anchor and a secondary anchor, said primary anchor having concave and convex parts and said secondary anchor being formed on the convex areas of said roughened surface.

54 (New). The printed circuit board according to Claim 24, wherein said electroless plated film is formed from an electroless plating solution comprising tartaric acid or a salt thereof.

55 (New). The printed circuit board according to Claim 24, wherein said via holes have a diameter of 80 μm or less.

56 (New). The printed circuit board according to Claim 25, wherein said electroless plated film comprises an alloy of copper and at least one metal species selected from the group consisting of nickel, iron and cobalt.

57 (New). The multilayer printed circuit board according to Claim 32, wherein said conductor circuit on said core board is a conductor layer interconnected with a plated-through hole.